TN126

JITTER TESTING OF PDM DEVICES

- [ ] 2700 Series
- [x] APx555
- [x] APx585 Series
- [x] APx525 Series
- [x] APx515

by Steve Peterson

Introduction

This Technote is intended for those involved in design and test of devices with Pulse Density Modulation (PDM) interfaces. It requires an Audio Precision APx analyzer with the APX-PDM option module (model 228), APX-AMC Advanced Master Clock, and APx500 software version 4.2 or later.

We will focus on jitter and related audio tests of PDM-interfaced integrated circuit components such as MEMS microphones, low-power amplifiers, and audio processors intended for mobile products such as smartphones, tablets, notebook computers, and wearable devices.

We will first review the fundamentals of PDM and jitter, the APx PDM interface, and the APx jitter generator and analyzer. Our focus will then shift to testing jitter tolerance of a MEMS microphone and a PDM class D amplifier, and configuring the PDM interface for jitter testing in APx Sequence Mode.

What is PDM?

PDM is best summarized as “oversampled 1-bit audio.” It’s a high sampling rate, 1-bit digital system.

For example, if you increased the sample rate of CDs by a factor of 64 (referred to as “oversampling”), and reduced the word length from 16 bits to 1 in a reasonable way, you’d have the basis of a PDM system.

An undithered 16-bit system has a theoretical signal-to-noise ratio of around 98 dB. An undithered 1-bit system has a signal-to-noise ratio of about 8 dB. However, the performance of a 1-bit system can be very high, using oversampling to provide increased bandwidth above the audible band (>20 kHz). Noise shaping in conjunction with oversampling moves the noise above the audible band.

PDM is implemented as a two-wire digital bus consisting of a bit clock signal and a data signal. A PDM bitstream is a logic-level data signal typically switching at around 3 MHz, with fast edges. Two channels of audio data may be encoded by clocking each channel on either a rising or falling edge of the bit clock.

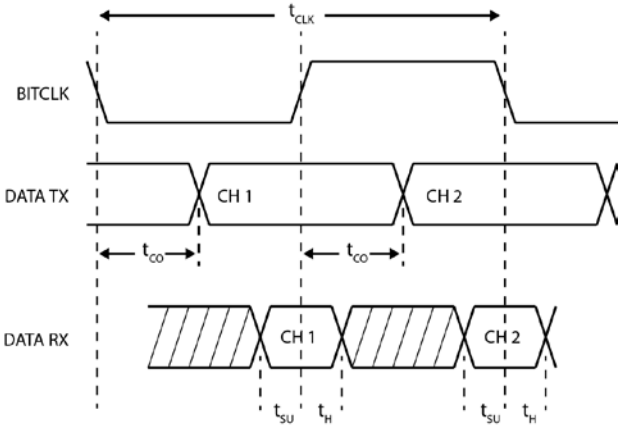


Figure 1. Two-wire PDM interface timing diagram.

Converting PDM to analog is very simple in principle. The oversampled, noise-shaped 1-bit signal on the data line already contains the audio in the low part of the spectrum. All that is required to recover it is a low-pass analog filter, but in practice the fast switching edges in the signal require careful design of the analog filtering stages.

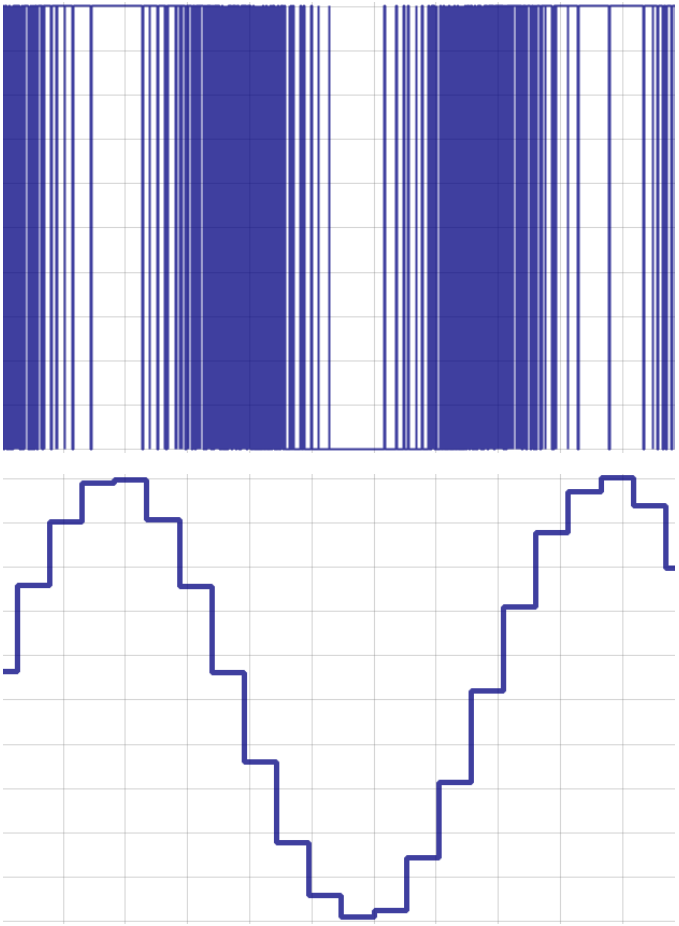


Figure 2. PDM bitstream (upper) and audio (lower).

Figure 2 shows a PDM data bitstream time synchronized with the decimated full-scale sine wave audio signal recovered from it. The pulse density modulation is visible; digital ones (1) correspond to full scale audio positive peaks and digital zeros (0) correspond to full scale negative audio peaks.

For an in-depth discussion of PDM technology, read the paper "Understanding PDM Digital Audio," available for download at ap.com.

What is Jitter?

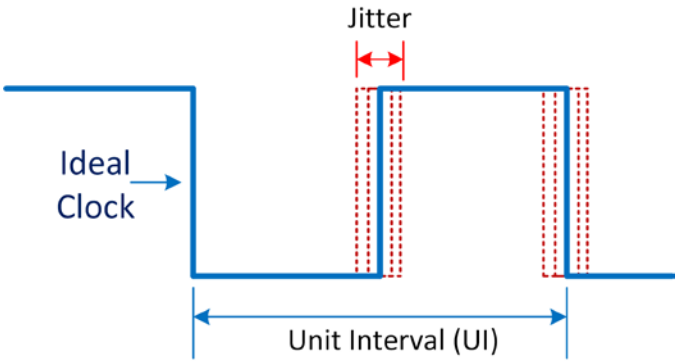


Figure 3. Jitter visualization.

Jitter is the variation in the time of an event—such as a regular clock signal—from nominal. For example, the jitter on a regular clock signal is the difference between the actual pulse transition times of the real clock and the transition times that would have occurred had the clock been ideal and perfectly regular. Against this nominal reference, the zero-crossing transitions of many of the pulses in a jittered data stream are seen to vary in time from the ideal clock timing. Jitter amplitude, then, is a measure of time displacement and is expressed in units of time or unit intervals (UI, the period of one bit clock interval).

The jitter component can be extracted from the clock as a signal for analysis. Among the more useful ways of characterizing jitter are examination of the jitter frequency spectrum, and identification of the significant frequency components of the jitter.

The APx PDM Interface

Audio Precision's PDM interface module is available for the APx555, APx52x Series and APx58x Series analyzers. It features both a PDM transmitter and an independent PDM receiver.

Figure 4. APx PDM hardware interface.

The APx PDM interface features:

- Independent transmitter output and receiver input supporting two channels of audio data on specified data clock edges.
- Variable logic levels from 0.8 V to 3.3 V.
- Bit clock rates from 128 kHz to 24.576 MHz.
- Sample rates from 4 kHz to 216 kHz.
- Vdd supply from 0.0 to 3.6 V with 15 mA current capability.
- 4th and 5th order modulators with optimization for oversampling rates of 32x, 64x, 128x, and 256x and automatic optimization for all other oversampling ratios.
- SNR of 129 dB.
- THD+N of −129 dB.
- Dynamic Range of 137 dB.
- Amplitude frequency flatness of ±0.0001 dB.
- Sine wave, square wave, and white noise jitter generation.
- Sine and square wave jitter generation from 2 Hz to 200 kHz.
- Jitter measurement range from 0 ns to 650 ns,50 Hz to 150 kHz.
- Peak, rms, or average jitter measurement detection.

The APx software provides control of the PDM module:

- Software user interface and programmatic control over physical interface parameters: logic and Vdd voltages, sample rate, data edge (mono and stereo edge selection), bit clock direction, generator modulator order (4th or 5th), generator oversampling ratio, 33 generator interpolation ratios (16–800x), and 45 analyzer decimation ratios (1–800x).
- Generation and analysis is in the digital domain to achieve high accuracy (no analog conversion).
- FFT analysis of the undecimated PDM bitstream or the decimated audio. The PDM bitstream mode measures the undecimated PDM spectrum up to 3.072 MHz (maximum 6.144 MHz input bit clock).
- Single or swept frequency Power Supply Rejection measurements utilizing the PDM module's built-in Vdd power supply output.
- Vdd power supply ramps from 0.0 V to 3.6 V for startup transient testing.
- Cross domain and cross interface measurements, combining the PDM input or output with any of the analyzer outputs or inputs: analog balanced, analog unbalanced, digital balanced (AES3), digital unbalanced (SPDIF), digital optical (TOSLINK), serial digital, HDMI, *Bluetooth* ™, and ASIO. Some interfaces are options and are not present on all instruments. PDM output with PDM input may also be configured.
- A comprehensive set of audio and jitter measurements.

APx Analyzer Options Required for PDM Jitter Measurements

Jitter measurements are available with APx analyzers configured with the Advanced Master Clock option.

The Advanced Master Clock module provides the jitter generator and jitter analyzer hardware that operates in conjunction with jitter-enabled APx digital hardware options, such as the PDM, ADIO (Advanced Digital Input/Output) and DSIO (Digital Serial Input/Output).

These interfaces and the Advanced Master Clock option can be added to existing APx Series audio analyzers (except the APx515).

APx PDM Output Settings

The PDM output is provided on the left side of the PDM module, data on top and bit clock on bottom (Figure 4). The PDM **Output Settings** panel (Figure 5) controls the bit clock direction and PDM data formatting parameters.

PDM input and output share the common **Logic Level, Vdd Level, Limit Logic Level,** and **Vdd On/Off** controls.

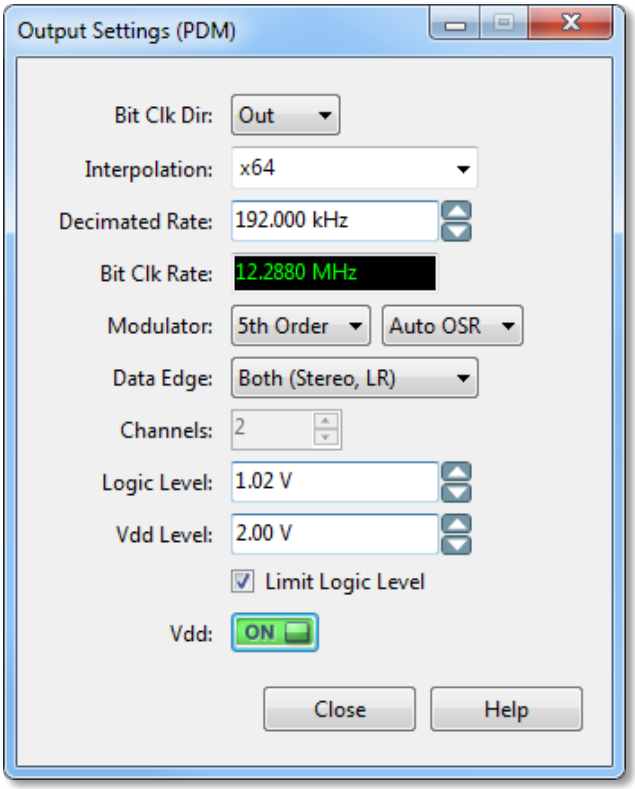


Figure 5. PDM transmitter Output Settings

APx PDM Input Settings

The PDM inputs are provided on the right side of the PDM interface module (Figure 4). The PDM Input Settings panel (Figure 6) controls the bit clock direction, PDM input data parameters, and shared output settings controls.

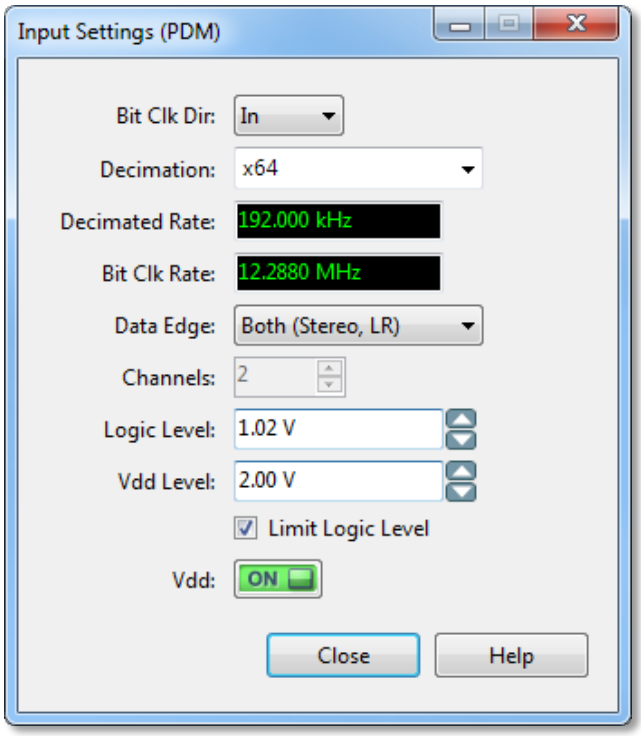


Figure 6. PDM receiver Input Settings

PDM Jitter Tests

Jitter tests of a PDM device measure the tolerance of the device to input clock jitter. Most PDM components are designed with the assumption that the clocks will have no significant jitter and therefore do not need to tolerate significant levels of jitter.

However, jitter on clock sources in mobile devices is likely, due to crosstalk from multiple digital busses and induced noise caused by high levels of near-field RFI from wireless transmitters (WiFi, Wireless Mobile, *Bluetooth* ™, NFC). Jitter on PDM bit clock and data lines may affect the audio performance of a PDM device, whether it is a MEMS microphone, class D amplifier, or a DSP processor with converters and inputs from PDM microphones and outputs to PDM amplifiers. Jitter may also be present on I²S audio buses connected to such devices.

PDM MEMS Microphone Jitter Tolerance Tests

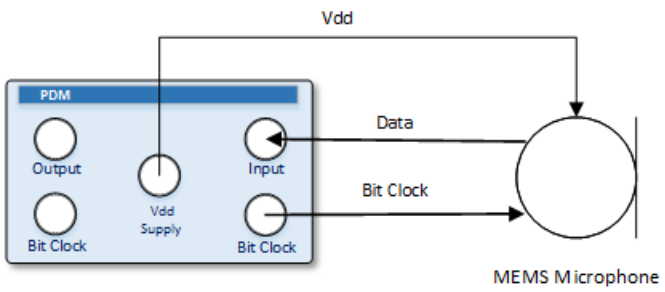


Figure 7. MEMS microphone test set-up.

In order to test a MEMS microphone component for jitter tolerance, stimulate the microphone with a low distortion acoustic sine wave tone in an acoustic test chamber. You can produce the signal with the APx analog or digital generator through an amplifier and speaker. Alternatively, a sine wave analog electrical signal may be applied by the APx analog generator directly to an integrated circuit with probes.

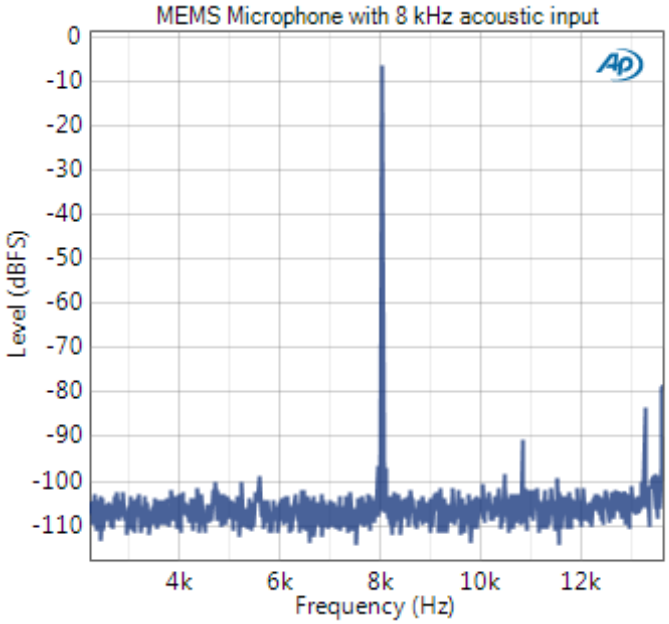


Figure 8. Normal MEMS microphone PDM audio spectrum with no applied bit clock jitter.

Figure 8 above illustrates normal operation of a MEMS microphone with an 8 kHz acoustic input test signal with no jitter applied to the bit clock input (Figure 7).

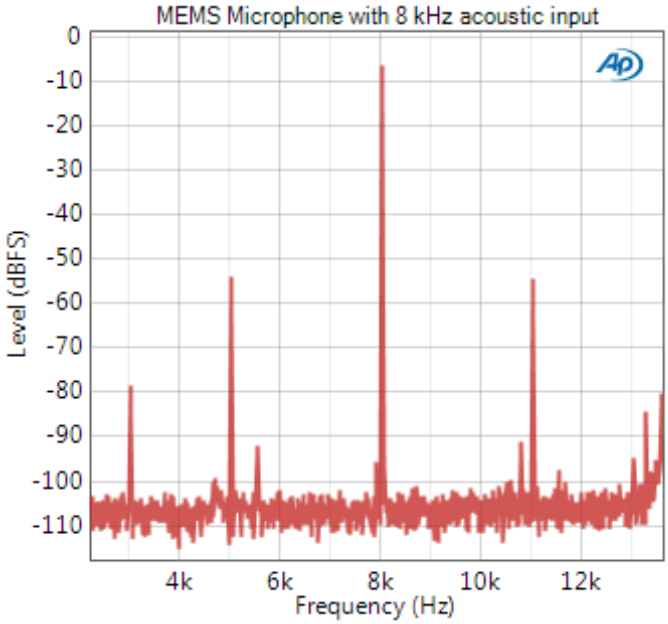


Figure 9. MEMS microphone PDM audio spectrum with 3 kHz sine wave bit clock jitter applied.

Jitter on the PDM clock line affects the audio performance of a MEMS microphone, resulting in audio modulation sidebands in the PDM audio data stream. This can be measured with an FFT spectrum or a THD+N meter.

If 3 kHz sine wave jitter is applied to the MEMS microphone bit clock input by the APx PDM input bit clock out (Figure 7), interference side bands are produced in the MEMS microphone audio data stream centered on the 8 kHz test signal, evident at 3 kHz, 5 kHz, and 11 kHz in Figure 9 above.

These frequencies were selected to illustrate the effects of jitter, but the principle applies to any frequencies within the normal operating range of the microphone.

MEMS Microphone Stepped Jitter Level Measurements

MEMS microphone jitter tolerance may be profiled with a stepped jitter level measurement with either sine wave jitter or noise jitter. In this test, THD+N distortion is measured for each increment of sine wave jitter amplitude stepped from 0 µs to 1 µs.

This can be easily setup with the APx analyzer **PDM Input Setting Panel** (Figure 10), **Clocks** Panel (Figure 11), **and Jitter Level Sweep** measurement (Figure 12).

1. On **the PDM Input Settings** Panel (Figure 10)
   a. Set **Bit Clk Dir** to **Out**.
   b. Set **Logic Level** and **Vdd Level** as required for the MEMS microphone, typically 1.8 V and 3 V respectively. **Logic Level** limits the maximum bit clock rate; set this before setting **Decimation** and **Sample Rate**.
   c. Set **Decimation** and **Sample Rate** as required for the MEMS microphone, typically **x64** and **48 kHz**. These settings interact with **Logic Level**.
   d. Set **Vdd** to **ON**. This applies power to the MEMS microphone, if supplied by the APx PDM interface.
   e. Set **Scale Freq By** to **Fixed Rate**, **48 kHz**. This turns off automatic frequency scaling in the PDM input and stabilizes notch tuning in the PDM analyzer. Automatic frequency scaling is not desired during jitter testing because it is accomplished by measuring the PDM data line input sample rate, which could vary when bit clock jitter magnitudes are large.

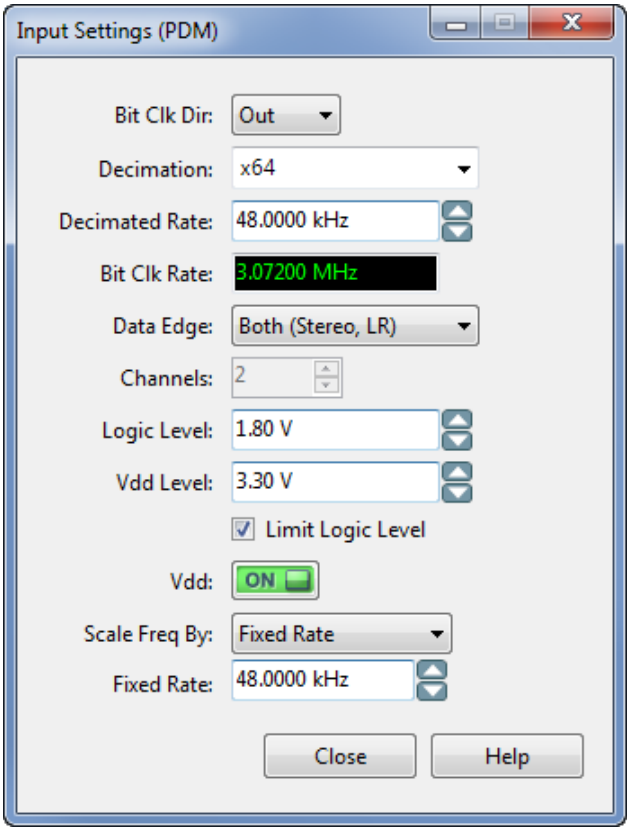


Figure 10. PDM Input Settings Panel configured for MEMS microphone tests.

2. On the **Clocks** Panel (Figure 11), **Jitter Generator:**
   a. Select **Digital Input** for **the Apply To** setting. This causes jitter to be applied to the PDM input receiver bit clock output.
   b. Set **Jitter Waveform** to **Sine.**
   c. Set **Jitter Frequency** to **10 kHz.**
   d. Set **Jitter Peak Level** to **0.0 s**.

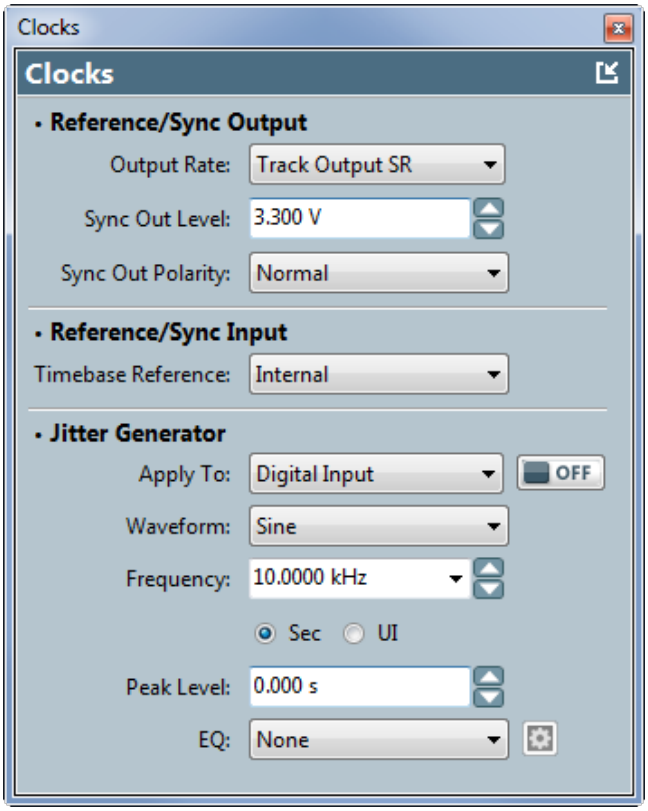


Figure 11. APx Clocks panel setup to jitter the output bit clock on the PDM input connected to a MEMS microphone.

3. Perform a **Jitter Level Sweep** in Sequence Mode (Figure 12).

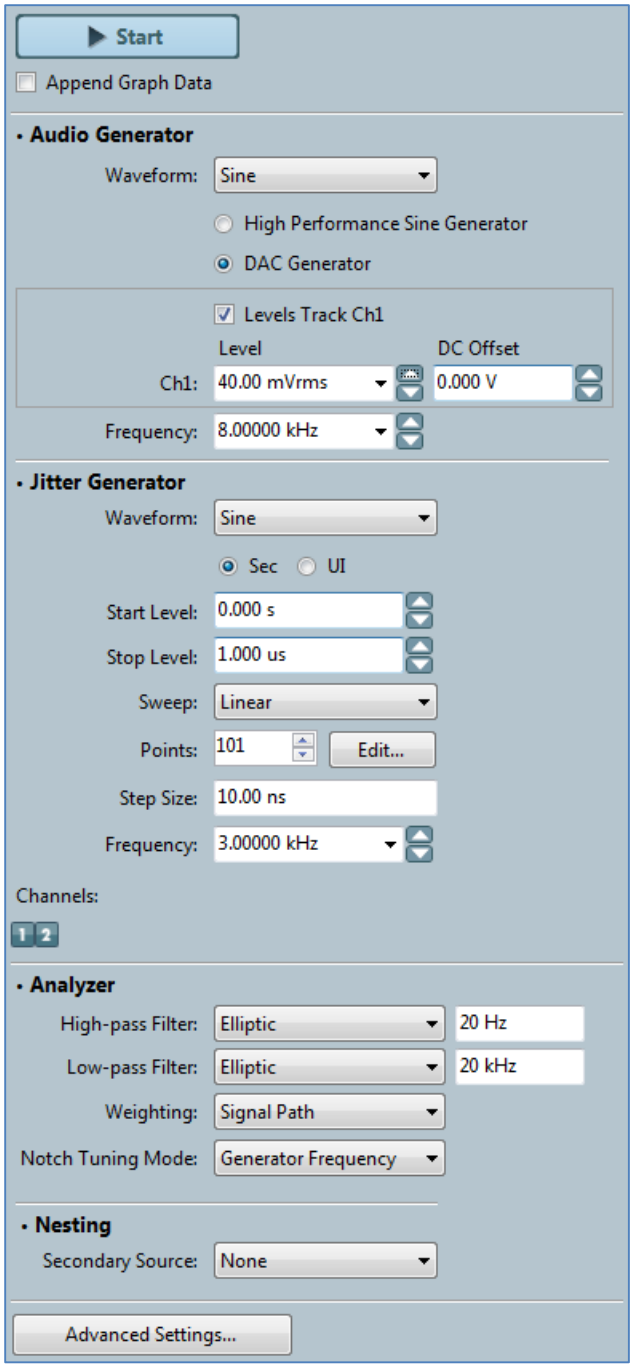


Figure 12. Jitter Level Sweep measurement settings for MEMS microphone jitter tolerance testing.

a. Set the analog audio generator level to drive the amplifier/loudspeaker sound field level to the MEMS microphone that produces a −10 dBFS PDM output. In this example, an unbalanced analog output level of 40 mV was applied to a speaker amplifier to produce the desired acoustic level at the MEMS microphone.
b. Set the audio sine wave **Frequency** to **8 kHz**.
c. Set the **Jitter Generator** sweep parameters to sweep from **0.0 s** to **1 µs** in **10 ns** steps at a jitter frequency of **3 kHz**.
d. Select the **THD+N Ratio** measurement result graph to view the result.
e. Start the sweep.

The choice of audio stimulus frequency and sine wave jitter frequency will result in different distortion curves depending on the frequencies involved. The 8 kHz audio frequency and 3 kHz sine wave jitter frequency was selected here to show the correlation between measured THD+N distortion and the spectrum shown in Figure 9.

As shown in Figure 13 below, audio distortion increases linearly as bit clock jitter level increases. The audio distortion increase is not surprising because the bit clock jitter is substantial. The MEMS microphone continues to function with up to 1 µs of bit clock sine wave jitter.

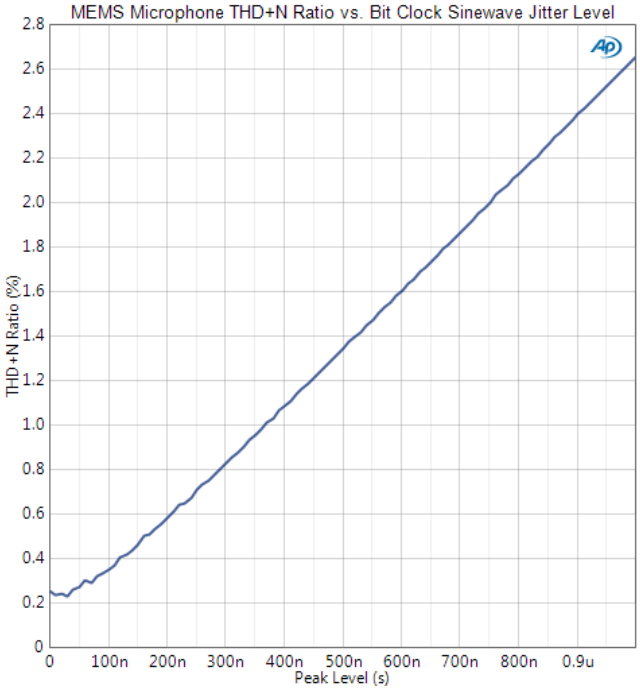


Figure 13. PDM MEMS microphone output THD+N as a function of stepped bit clock sine wave jitter level.

MEMS Microphone Stepped Jitter Frequency Measurements

Sine wave jitter frequency sweeps may also reveal interesting behaviors in MEMS microphones.

Figure 14 below shows a graph of a MEMS microphone output THD+N distortion (with a 10 kHz acoustic sine wave stimulus) as a function of bit clock jitter frequency at a fixed 1 UI jitter level (325.5 ns at 3.073 MHz bit clock rate, 48 kHz audio sample rate, x64 decimation).

The THD+N distortion measurement detects interference signals caused by the PDM bit clock jitter by eliminating the audio fundamental with a notch filter and measuring all remaining in-band signals.

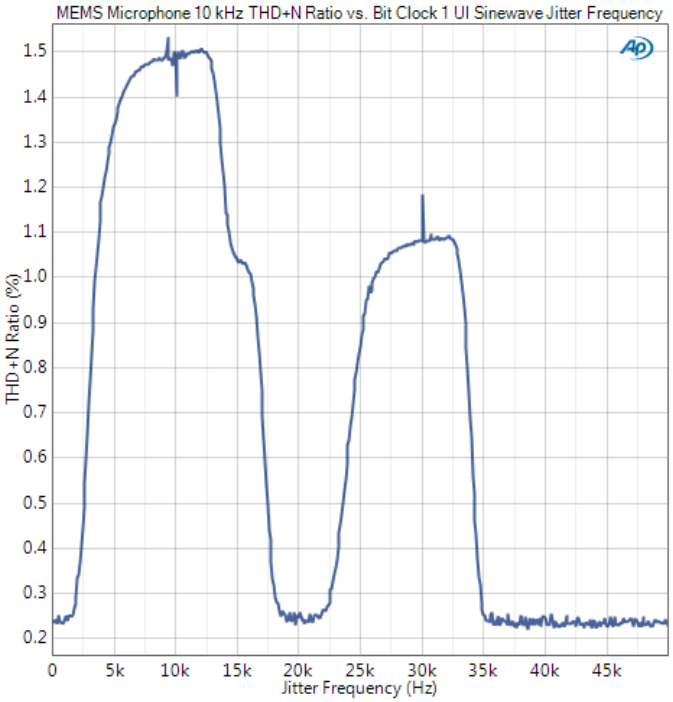


Figure 14. PDM MEMS microphone output THD+N as a function of stepped bit clock sine wave jitter frequency.

In this particular MEMS microphone, the jitter frequencies above the 24 kHz folding frequency generate significant in-band interference measured as high THD+N distortion.

The settings for this Jitter Frequency Sweep measurement are shown in Figure 15. The sweep settings start the jitter frequency sweep at 50 kHz and stop at 20 Hz. The choice of sweep direction is arbitrary.

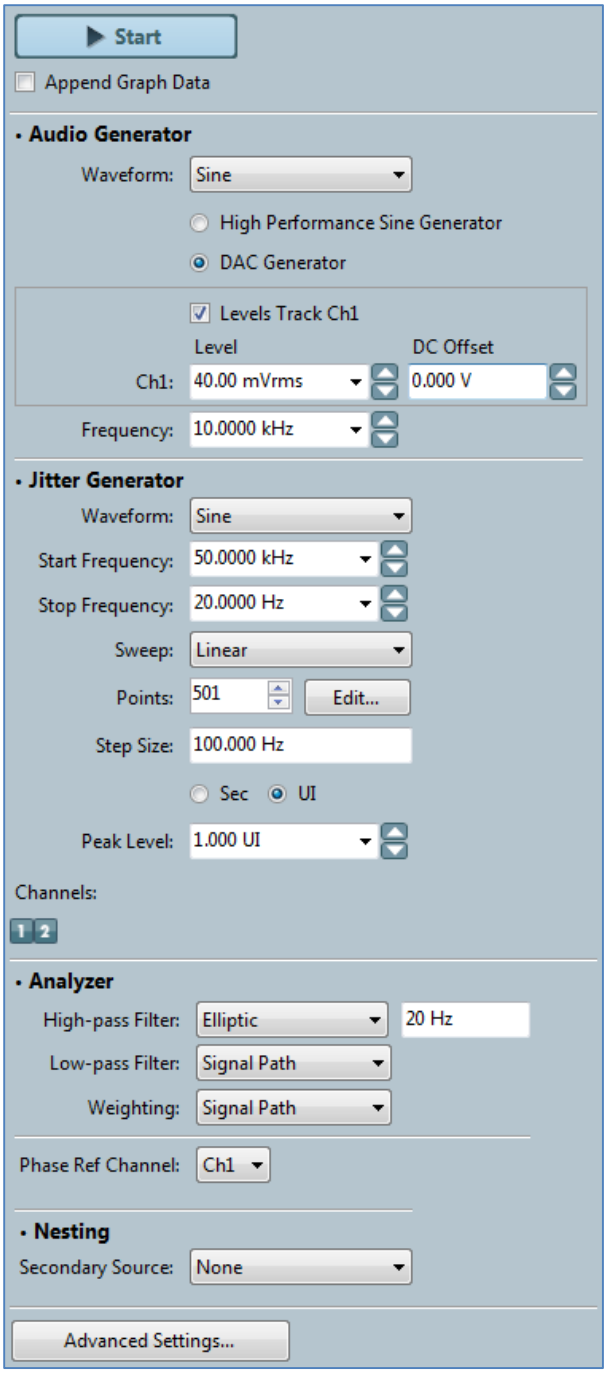


Figure 15. MEMS microphone Jitter Frequency Sweep settings.

Nested Stepped Jitter Sweep Measurements

The jitter frequency sweeps and jitter level sweeps can be combined to produce a family of curves within one measurement graph. APx supports this with sweep nesting, a feature of the Jitter Level Sweep, Jitter Frequency Sweep, Acoustic Response, Continuous Sweep, Frequency Response, and Signal Analyzer measurements in Sequence Mode. Bench Mode supports nested sweeps for all measurement types.

Figure 16 illustrates this with a Jitter Frequency sweep for each nested Jitter Level, while measuring a MEMS microphone PDM output THD+N Ratio distortion with a constant acoustic input. This Jitter Frequency Sweep steps sine wave jitter frequency in 100 Hz increments from 50 kHz to 20 Hz at 6 different jitter levels. Each color-coded jitter level is noted in the legend.

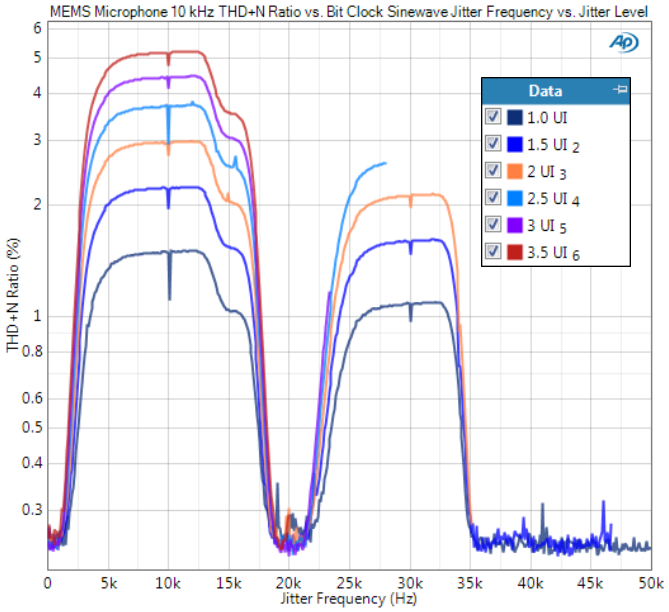


Figure 16. PDM MEMS microphone bit clock jitter frequency sweep as a function of jitter level (nested sweep).

Figure 17 shows the APx measurement panel settings to accomplish this nested jitter sweep. The **Nesting** section of the panel controls the jitter level secondary source parameters.

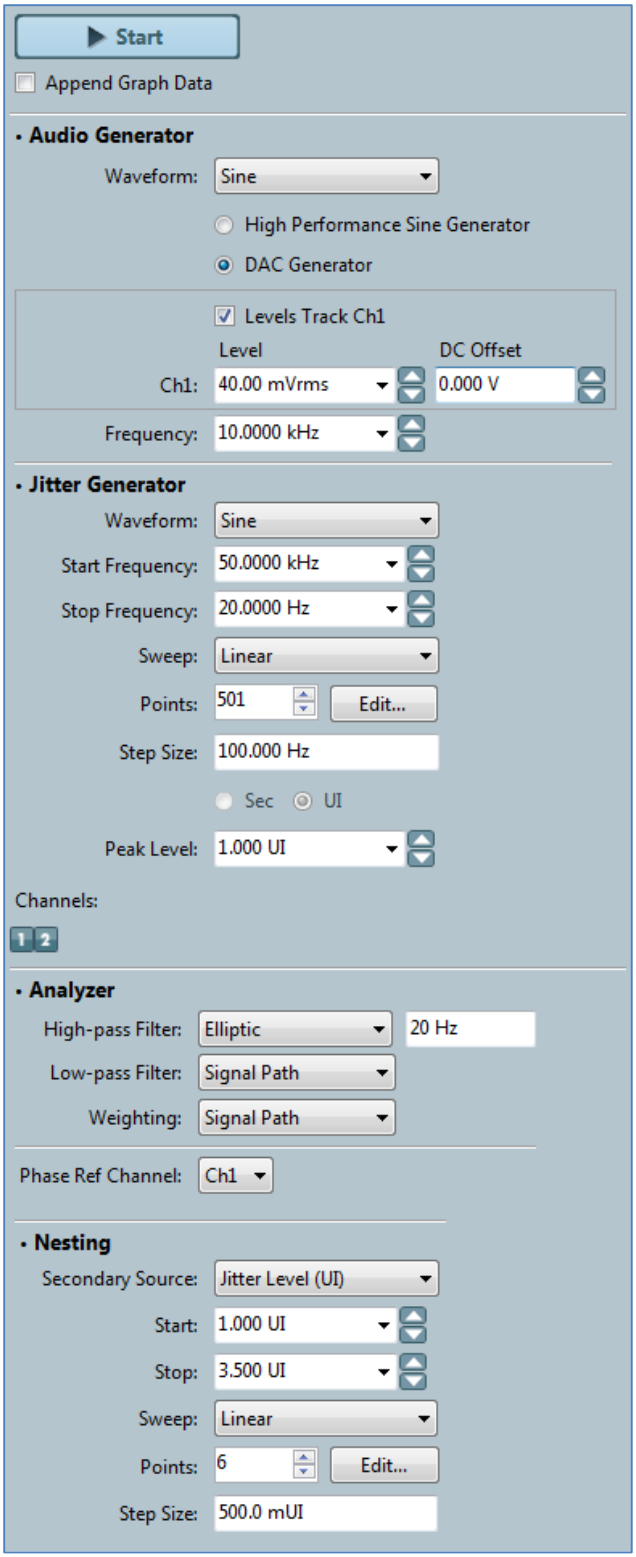


Figure 17. MEMS microphone nested jitter frequency and jitter level sweep setup.

PDM Amplifier Jitter Tolerance Tests

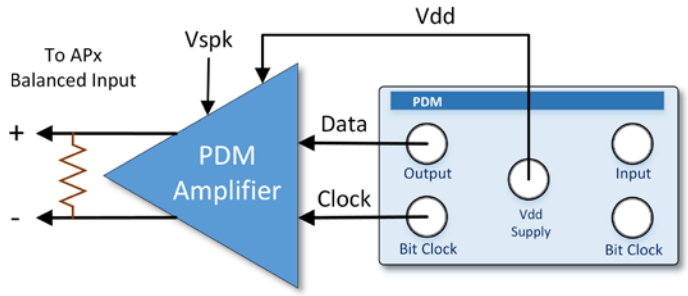


Figure 18. PDM amplifier test connections.

PDM amplifier jitter tolerance measurements are accomplished by driving the amplifier with a jittered PDM signal while measuring normal amplifier output performance with a resistive load.

The PDM audio input level should be set to achieve 50% rated output power (3 dB below the 1 kHz audio sine wave rms level that results in 1% THD+N output distortion). This output level assures the jitter tolerance is measured within the normal operational range of the amplifier.

The PDM class D amplifier used for these measurements was setup to operate at a 48 kHz sample rate with x128 interpolation, resulting in a 6.144 MHz bit clock rate.

For details of how to measure power amplifiers with APx analyzers, please see the References section at the end of this Technote.

Noise Jitter Tests

Noise Jitter on the PDM bit clock and data lines of a class D amplifier causes an increase in output noise and harmonic distortion, measurable with level and distortion meters.

Noise Jitter Level Sweeps

Jitter tolerance can be measured with a sweep of PDM input white noise jitter level while measuring amplifier output THD+N distortion.

APx software performs this measurement with a fixed PDM audio output signal while running a Jitter Level Sweep. This measures the amplifier output THD+N distortion at each jitter level. The result is a plot of degraded amplifier distortion versus jitter level. Distortion increases linearly as noise jitter level increases from 0 to 0.246 UI (40 ns), shown in Figure 19.

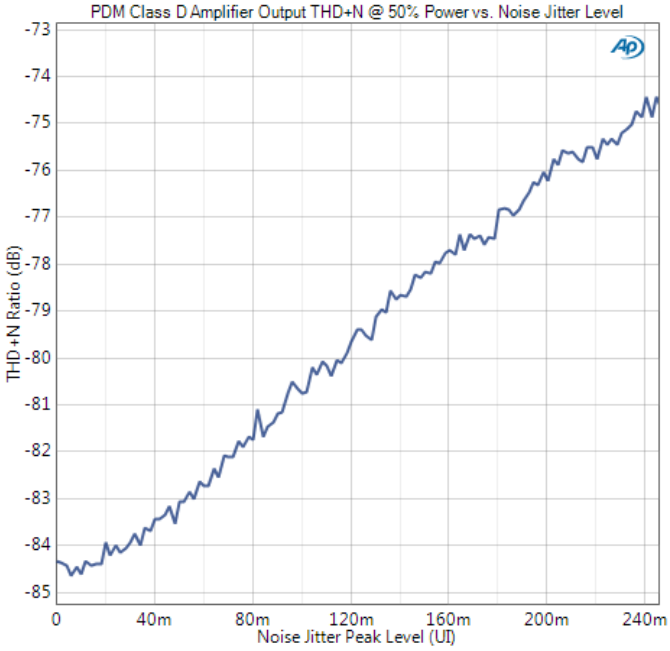


Figure 19. PDM class D amplifier output distortion versus PDM input noise jitter level.

Output Distortion vs. Output Power vs. Jitter Level

Another method to investigate the effects of noise jitter on amplifier performance involves measurements of output distortion as a function of output power with and without noise jitter.

The graphs in Figure 20 show this with sweeps of the amplifier's audio input level while measuring output power and output distortion, performed with and without 0.246 UI (40 ns) noise jitter applied to the PDM input. Sweep measurements are performed with and without jitter and overlaid (appended data sets) on the same graphs.

The lower distortion blue curves are measurements without jitter. The higher distortion red curves are measurements with 0.246 UI noise jitter. The noise jitter increases both THD and THD+N distortion measurements by approximately 10 dB. The jitter affects harmonics and noise, notable by the fact that both THD and THD+N measurement curves shifted up and THD+N was 10 dB above THD in both cases.

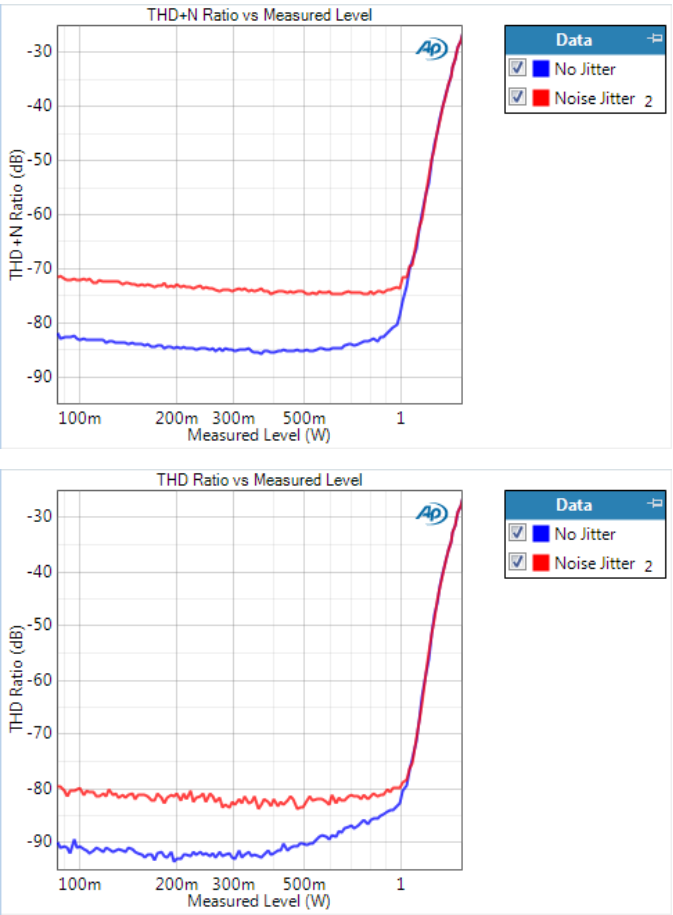


Figure 20. Class D PDM amplifier THD and THD+N vs. Output Power vs. Noise Jitter.

Sine wave Jitter Tests with Nested Sweeps

An alternative test of amplifier jitter tolerance may be performed with sine wave jitter with nested sweeps of jitter frequency and jitter level to produce a family of jitter tolerance curves.

Figure 21 shows the results of nested sweep jitter tests on the PDM class D amplifier with a 1 kHz audio test signal driving the output to 50% rated output power (750 mW for this particular amplifier). Audio bandwidth is limited to 20 kHz in order to measure distortion within the normal passband specified for this amplifier. Jitter frequency is swept from 20 kHz to 50 Hz for jitter level settings from 0 UI (no jitter) to 3.5 UI (0 to 569.7 ns at a bit clock rate of 6.144 MHz, 128x 48 kHz sample rate) in 0.5 UI steps (81.4 ns). Each curve is a jitter level.

The blue and red curves show normal amplifier performance with no jitter on the PDM bit clock. The other curves show increasing levels of audio output distortion as sine wave jitter increases in frequency for each jitter level.

Sine wave jitter produces modulation sidebands of the 1 kHz test tone fundamental and significant distortion harmonics. These modulation sidebands increase in level and change frequency as jitter frequency changes.

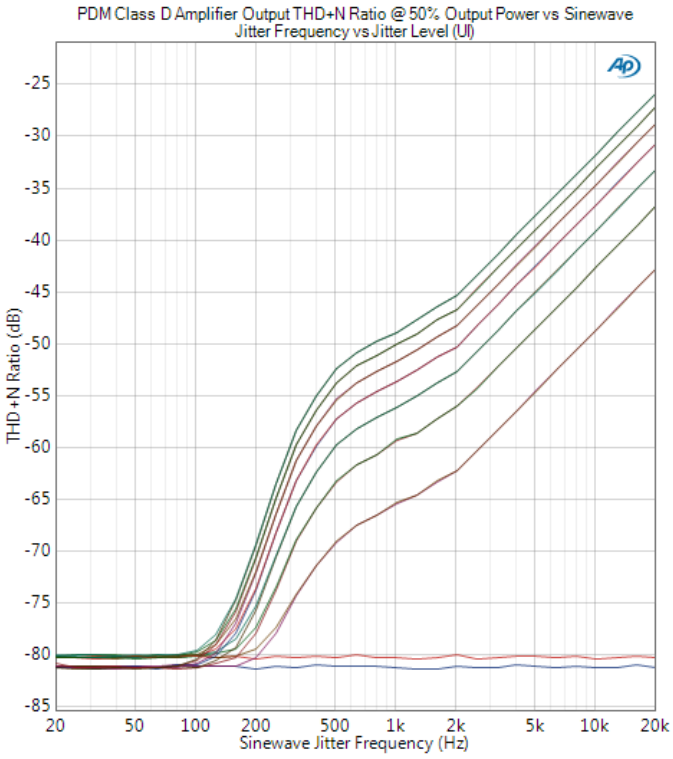


Figure 21. PDM class D amplifier distortion vs. PDM input sine wave jitter frequency versus jitter level 0 to 3 UI.

Setting up the Jitter Frequency Sweep – Nested Jitter Level Measurement

The **Jitter Frequency Sweep** measurement may be set up with the panel settings shown in Figure 22.

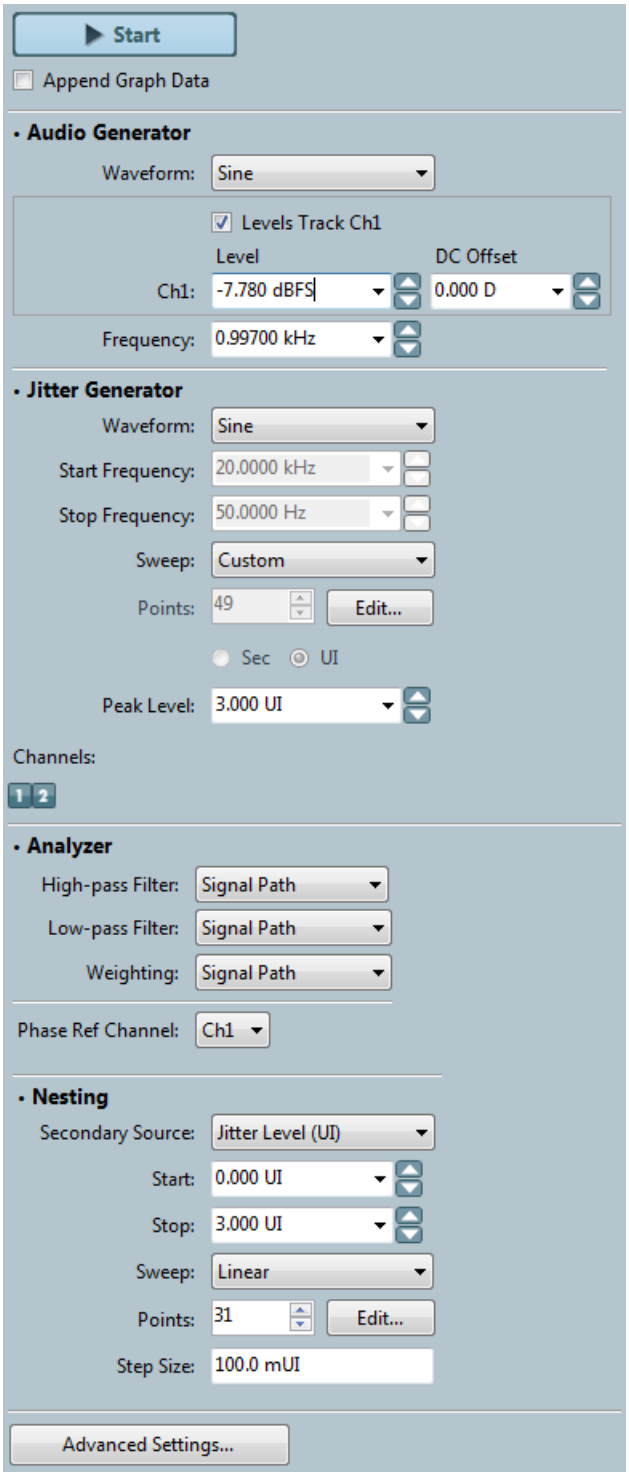
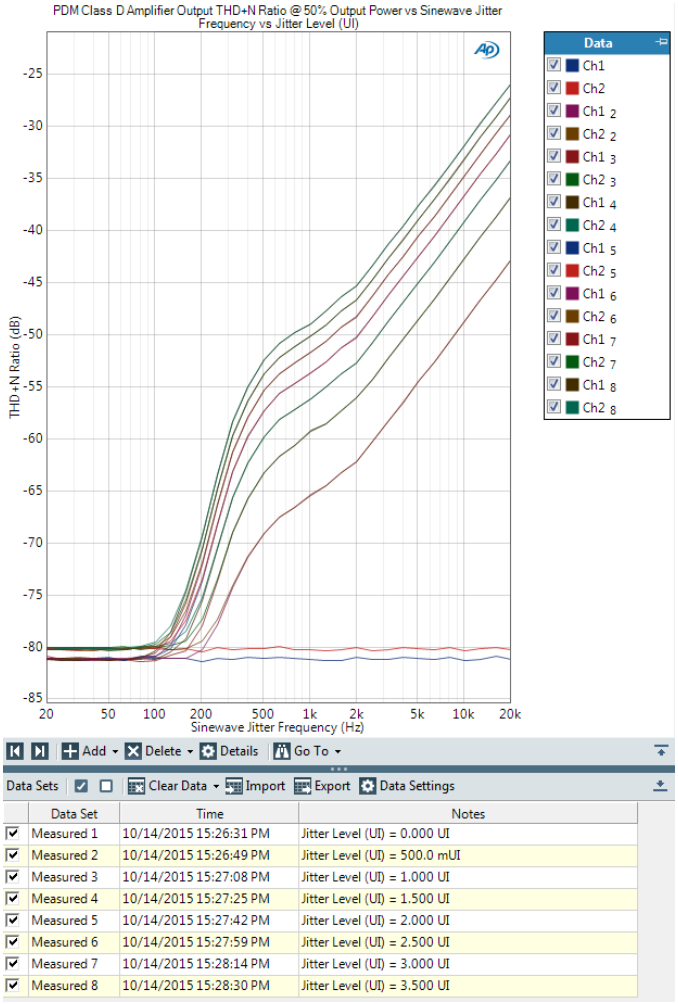


Figure 22. Jitter Frequency Sweep setup for PDM Class D amplifier testing.

The **Start** button begins the sweep and updates the graph and **Data Set** displays as it runs. Figure 23 below shows the final results graph (Figure 21) with the Data Sets display.

Each **Data Set** is an array of THD+N distortion measurements versus jitter frequency for a given jitter level, documented in the Notes column for reference.



Data Set	Time	Notes
Measured 1	10/14/2015 15:26:31 PM	Jitter Level (UI) = 0.000 UI
Measured 2	10/14/2015 15:26:49 PM	Jitter Level (UI) = 500.0 mUI
Measured 3	10/14/2015 15:27:08 PM	Jitter Level (UI) = 1.000 UI
Measured 4	10/14/2015 15:27:25 PM	Jitter Level (UI) = 1.500 UI
Measured 5	10/14/2015 15:27:42 PM	Jitter Level (UI) = 2.000 UI
Measured 6	10/14/2015 15:27:59 PM	Jitter Level (UI) = 2.500 UI
Measured 7	10/14/2015 15:28:14 PM	Jitter Level (UI) = 3.000 UI
Measured 8	10/14/2015 15:28:30 PM	Jitter Level (UI) = 3.500 UI

Figure 23. The Graph and Data Set displays show the nested sweep data.

Setting Up PDM Jitter Tests with APx

PDM jitter tests involve the interaction between PDM I/O settings, Clock panel settings, and analog I/O settings depending on the type of PDM device tested. These settings are available in the Signal Path Settings for each signal path.

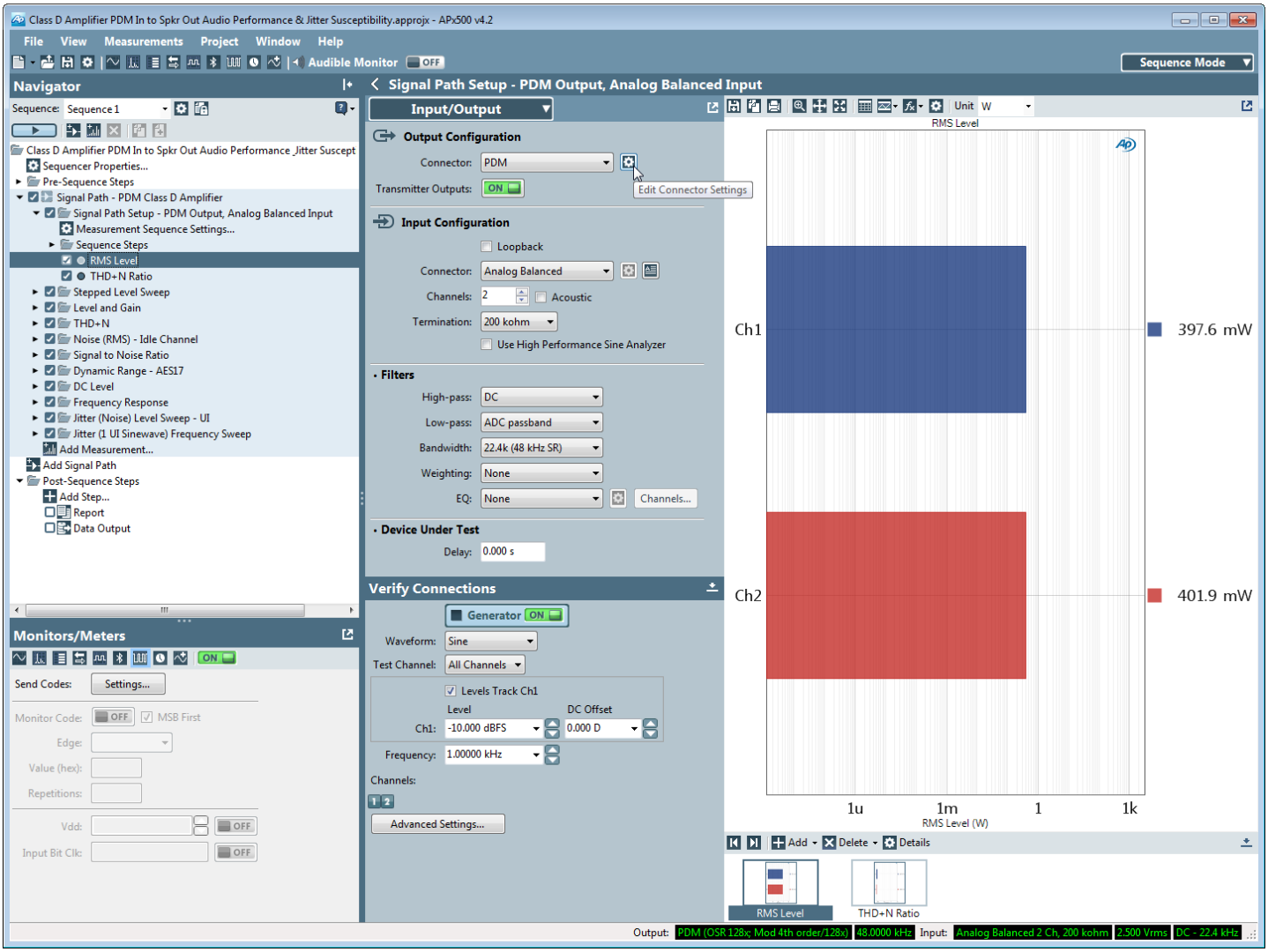


Figure 24. Sequence Mode setup for PDM Class D amplifier tests.

shows the Sequence Mode Signal Path Setup display with PDM Output Configuration and Analog Balanced Input Configuration settings appropriate for testing a PDM Class D amplifier.

PDM Jitter Generator Setup with the Clocks Panel

The **Clocks** panel is selected from the drop-down list box in **Signal Path Setup** as shown in Figure 25.

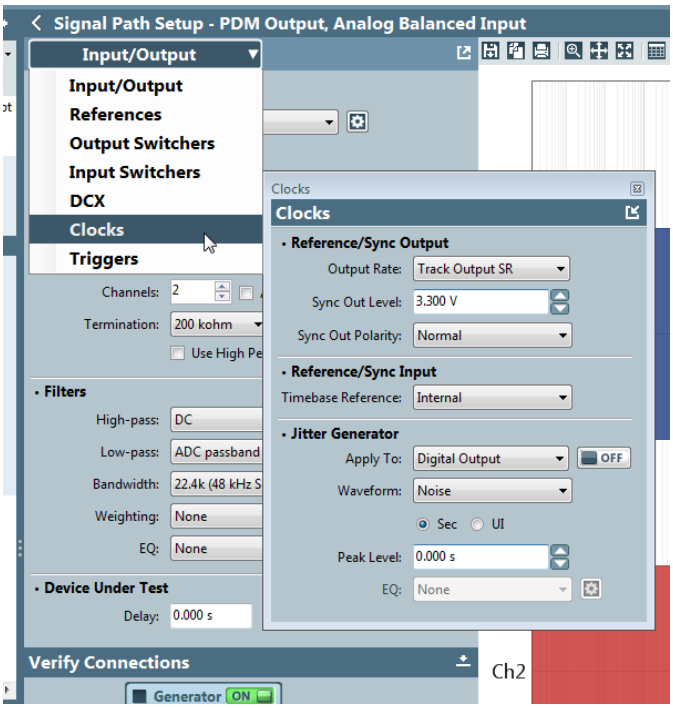


Figure 25. The Clocks panel accessed from the Signal Path Setup panel provides control of the Jitter Generator.

The **Jitter Generator** section of the clocks panel contains the controls for the jitter generator. This panel controls the optional Advanced Master Clock. The Advanced Master Clock (AMC) option is required to support jitter tests with the PDM module. The AMC provides jitter capability to four functional areas of the instrument:

- Rear-panel **Sync Out** and **DARS Ref Out**.
- Advanced Digital I/O (ADIO) module for AES-EBU/SPDIF/Optical.
- Clock lines of the Digital Serial I/O module DSIO) for I²S and other formats.
- Clock lines of the PDM module.

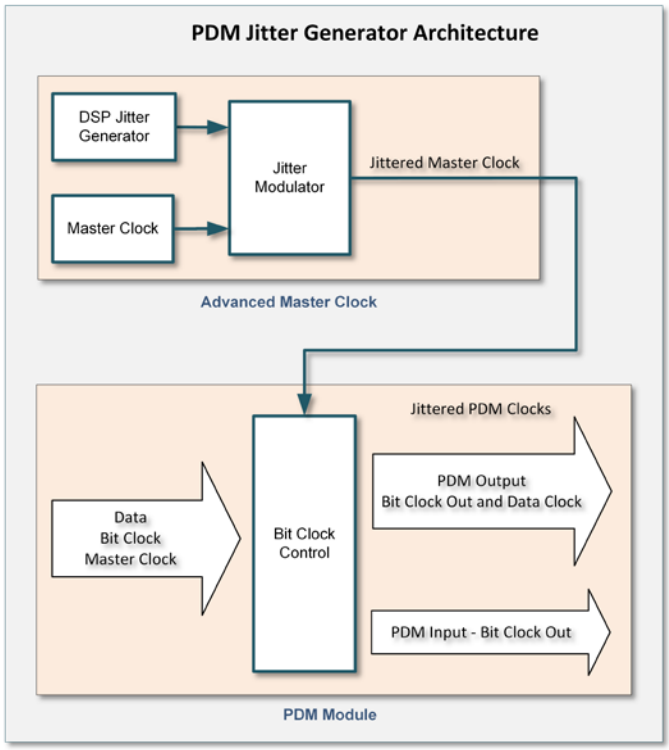


Figure 26. APx PDM Jitter Generator Architecture

As shown in Figure 26 above, the AMC jitter generator provides a jittered master clock to the PDM module, which then provides a jittered PDM transmitter bit clock output (and data) or a jittered PDM receiver bit clock output.

The jitter generator controls on the Clocks panel (Figure 27) provide control of source (Apply To), waveform type (sine, square, or noise), frequency (if waveform type is sine or square), and jitter amplitude in seconds or unit intervals. The jitter generator amplitude is calibrated in peak level seconds or UI (unit intervals relative to the bit clock period and scaling with bit clock rate).

Figure 27 shows the **Clocks** panel setup to produce 15 ns of peak level 1 kHz sine wave jitter to the PDM digital output transmitter bit clock, when PDM is selected as the active APx output and its Bit Clock is set to output.

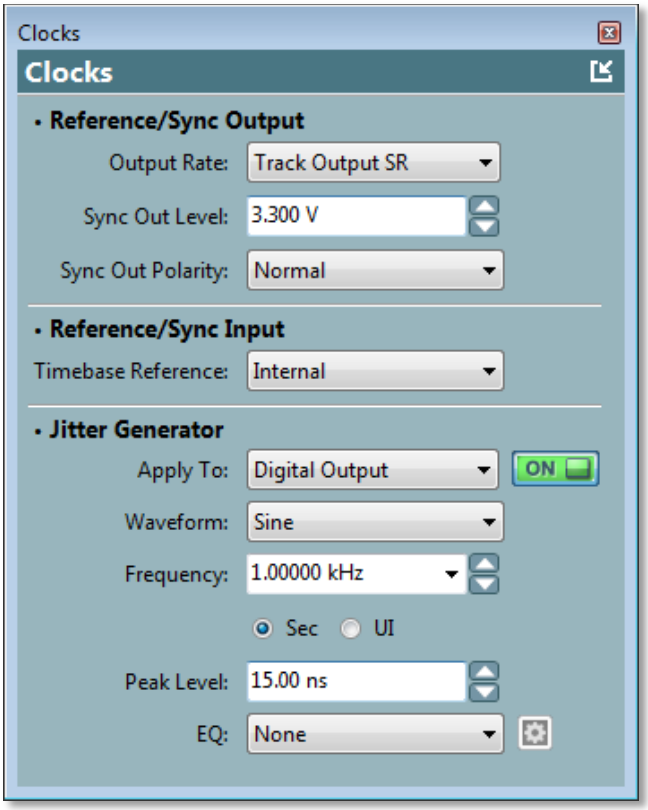


Figure 27. The APx Clocks Panel Jitter Generator Settings

PDM Jitter Analyzer Setup with the Input/Output Panel

Devices with PDM outputs may have jitter on their bit clock outputs, such as processors that source PDM signals to low-power PDM class D amplifiers in mobile phones. Jitter on the PDM output of the processor can be measured with the APx PDM receiver input using the Advanced Master Clock jitter demodulator and jitter analyzer.

The **Signal Path Setup Input/Output** panel displays a Measure control when the Advanced Master Clock module is installed, a jitter capable digital interface is selected for Input, and the input bit clock is a slave (input).

The **Measure** control defaults to **Audio**. Select either **Jitter (sec)** or **Jitter (UI)** to enable jitter measurements (see Figure 28).

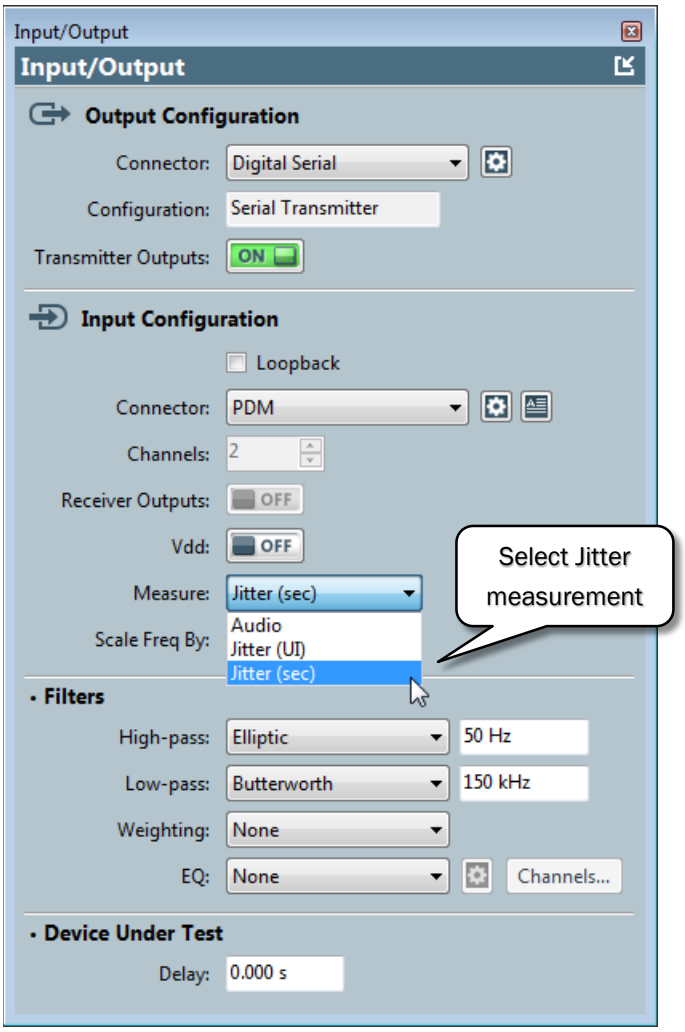


Figure 28. APx Input/Output panel configured for Jitter (sec) measurements.

Selecting one of the jitter choices enables the APx jitter analyzer. The block diagram in Figure 29 shows the internal architecture of the PDM module and jitter analyzer. The jitter analyzer demodulates the jitter on the PDM receiver bit clock input and provides a calibrated jitter signal to the APx measurement system.

When jitter is selected as the input in the Input/Output panel, the APx measurement system switches to the jitter demodulator instead of the PDM data stream, and all APx measurements are jitter measurements. Audio measurements are not available when jitter measurements are selected.

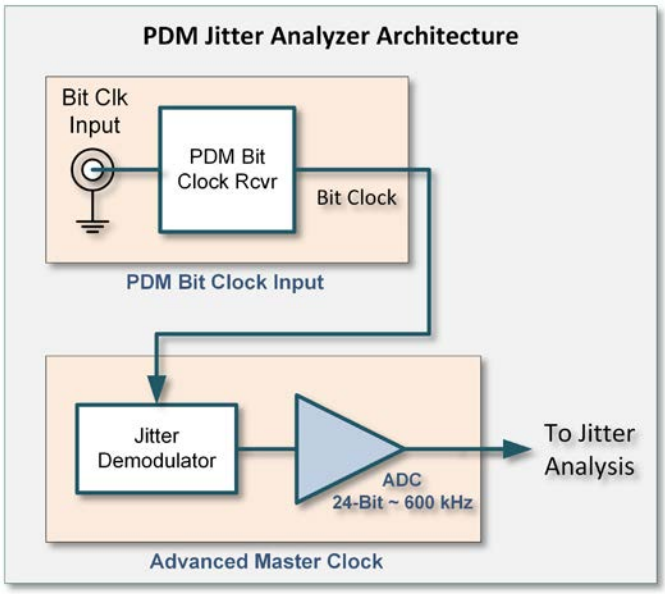


Figure 29. APx PDM Jitter Analyzer Architecture

Figure 30 below is an example of an APx jitter spectrum measurement of an audio hub IC PDM output.

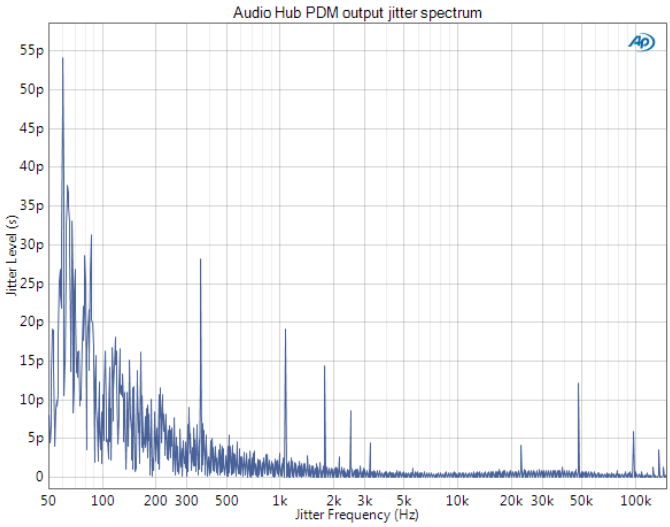


Figure 30. Spectrum of jitter on a PDM output of an audio hub IC.

Special Considerations

PDM Jitter Generator Derating

The PDM jitter generator sine wave output level derates with frequency above 20 kHz. This derating occurs automatically when jitter level or frequency is set when sine wave jitter is in use. The jitter level decreases at the rate of –6 dB per octave from 20 kHz to 200 kHz, as shown in Figure 31.

The curves represent the maximum jitter level at any given jitter frequency. The maximum jitter level at 1 kHz is 3.5 UI or 1.592 µs, whichever time interval is less.

For example, given a 1 kHz jitter signal at a bit clock rate of 6.144 MHz, a jitter level of 3.5 UI is 569.7 ns (3.5/6144000). The maximum 1.592 µs jitter level is not attainable, but 3.5 UI is. This principle applies to the derating curves.

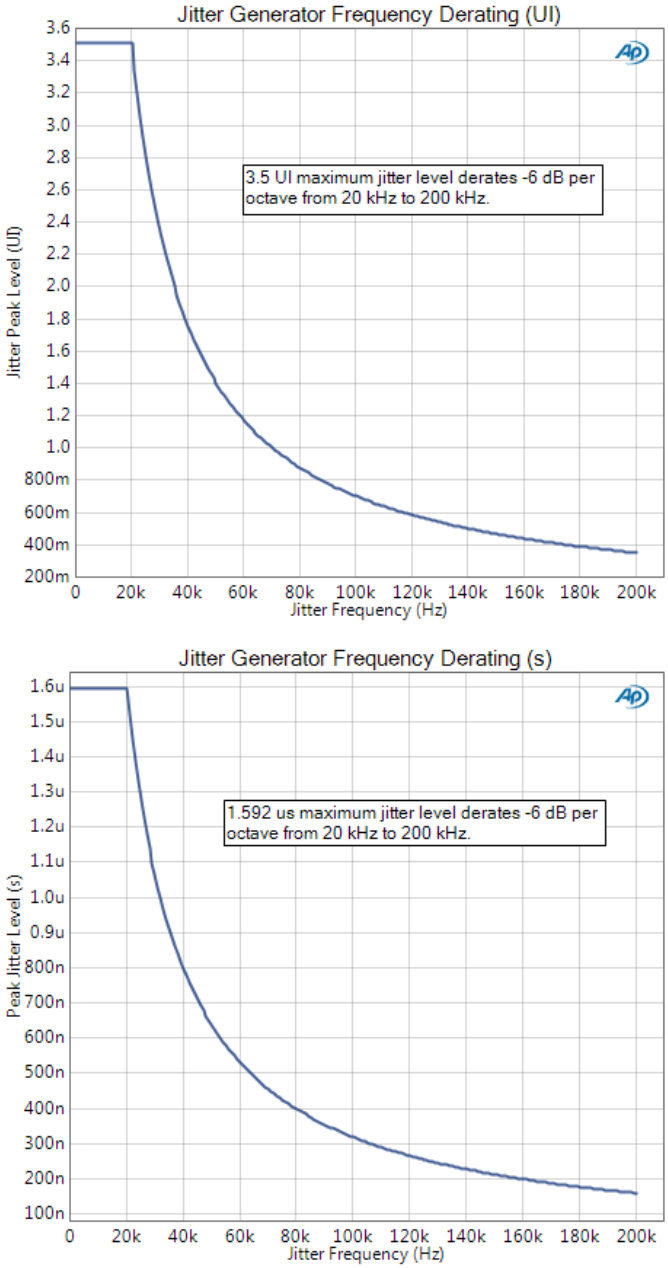


Figure 31. Jitter generator maximum sine wave jitter level in UI and seconds vs. jitter frequency.

Jitter Generator Derating in Jitter Level Sweep Measurements

Jitter Level Sweep measurements operate at a fixed jitter frequency setting unless jitter frequency is specified for a nested secondary sweep source. If a jitter level sweep specifies a jitter level value above the derating curve value for the fixed jitter frequency then all jitter level values above the curve will be skipped.

Jitter Generator Derating in Jitter Frequency Sweep Measurements

Jitter Frequency Sweep measurements will automatically track the jitter generator derating curve, and will decrease the jitter level when frequency exceeds the curve for a given jitter frequency setting. This can be seen while watching the Jitter Level control during the sweep. For example, during a jitter frequency sweep with jitter level set to 1 UI, the jitter level will decrease for jitter frequencies above 70 kHz, and a jitter level set to 455 ns would also decrease above 70 kHz.

Jitter Generator Derating in Nested Jitter Sweeps

A jitter frequency sweep can be configured with a nested jitter level sweep. In such a configuration, when the jitter frequency sweep runs for each nested jitter level specified and exceeds the limit of the jitter generator derating curve, then the sweep point will be skipped. The automatic jitter level derating will not occur because the jitter level is fixed during the jitter frequency sweep.

Figure 16 on page 9 illustrates this in a PDM microphone jitter frequency sweep with a nested jitter level sweep. The jitter frequency sweep is performed at the first jitter level of the nested jitter level sweep. The jitter level is fixed during that iteration of the jitter frequency sweep, and does not change to track the maximum level described by the jitter generator derating curves. In Figure 16, jitter frequency sweeps at higher nested jitter generator levels do not include all jitter frequencies specified in the jitter frequency sweep range. To demonstrate this, note that the jitter frequency maximum is only 28 kHz in the 2.5 UI nested sweep but is 23.3 kHz in the 3 UI nested sweep.

If you are not sure of the maximum jitter frequency possible for a given nested jitter level, you may set the jitter frequency sweep start or stop frequencies as desired, and the APx software will automatically skip the disallowed frequencies.

However, setting the start and stop frequencies both above the maximum frequency for any given jitter level will result in an error, shown in Figure 32. This can happen if the range of jitter frequency start and stop is invalid for one of the jitter level nested sweeps. If this happens the entire sweep will stop when the error occurs. To avoid this, start the nested sweep at the lowest jitter level in order to accumulate all measurements prior to the error (if any).

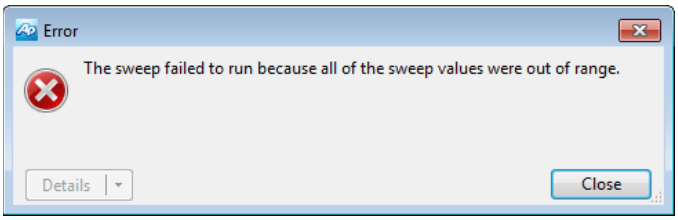


Figure 32. APx error display if jitter sweep values are above the maximum frequency or level.

Audio Frequency Scaling and Filter Tuning with Scale Freq By

The APx measurement system automatically tunes filters to track signal generator frequencies or measured frequencies. When the signal generator is a digital source and the analyzer is automatically tuning to its frequency, generator frequency is determined by scaling the audio according to the measured sample rate of the generator. This is desirable because it makes the system easy to use, requires no overt tuning on the part of the user, and tracks changing sample rates automatically.

However, when the signal source involves a clock signal with significant induced jitter for testing purposes, such as PDM, the process of generator sample rate measurement may produce incorrect or unstable audio frequency generation because of the jitter. This is not surprising, because jitter is a form of bit clock frequency modulation, which is sample rate modulation.

These jitter-induced frequency errors affect measurement filters in the analyzer and may cause incorrect or unstable measurements. This is especially noticeable with the tuned notch filters used in THD and THD+N measurements, and affects user-selected corner frequencies of high pass, low pass, and weighting filters in the analyzer.

The solution is provided with the Scale Freq By settings on the PDM Output Settings and PDM Input Settings panels (Figure 33 and Figure 34 on the next page). The normal settings are Decimated Rate and Input SR, respectively.

Choose **Fixed Rate** settings in order to specify the nominal sample rate. The **Fixed Rate** setting overrides the auto-sample rate audio scaling process and produces stable measurements in the presence of high clock jitter levels (on PDM bit clock output or measured PDM bit clock input).

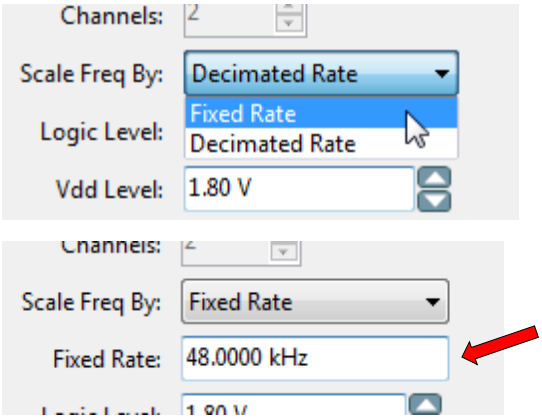


Figure 33. PDM Output Settings for Scale Freq By. The Fixed Rate sample rate control appears when Fixed Rate is selected.

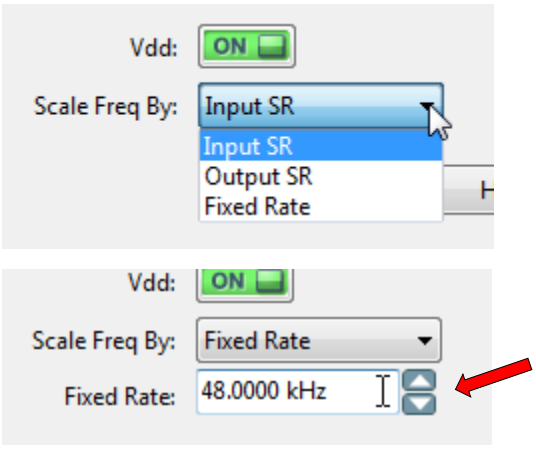


Figure 34. PDM Input Settings for Scale Freq By. The Fixed Rate sample rate control appears when Fixed Rate is selected.

PDM Clock Switching

The APx PDM interface hardware switches between the unjittered master clock and the jittered master clock (Figure 26 on page 14) according to the user-setting of the jitter generator On/Off control on the Clocks panel (Figure 27). Certain measurements in Sequence Mode automatically enable and disable the jitter generator. The PDM outputs momentarily stop when the jitter generator output is turned on or off, when the hardware switches between the two master clocks.

Clock switching will occur if the jitter generator is off in the **Clocks** panel in the **Signal Path Setup** but turned on later in a measurement sequence by **Jitter Frequency Sweep, Jitter Level Sweep**, and measurements configured with nested jitter sweeps**: Acoustic Response, Continuous Sweep, Frequency Response,** and **Signal Analyzer**. The momentary clock interruption may reset PDM devices that have been programmed with PDM control codes. This clock switch behavior can be managed within APx measurement sequences.

APx provides the Send PDM Control Codes sequence step to setup a PDM part for testing within a measurement. Figure 35 shows a **Jitter Frequency Sweep** measurement, in the Sequence Mode Navigator, with a **Send PDM Control Codes** sequence step just before the **Measure Jitter** step starts the jitter sweep.

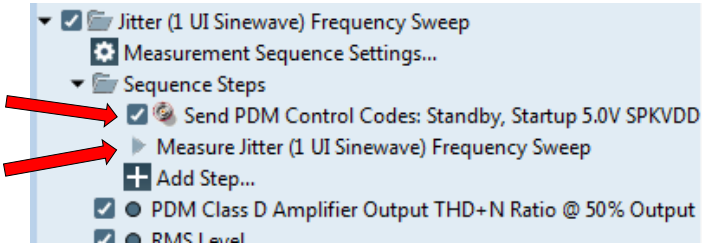


Figure 35. Jitter Frequency Sweep measurement in a Sequence, with Send PDM Control Codes sequence step.

This particular control code sequence sends the code 66 to put the part in Standby and code D8 to startup the amplifier for maximum output with a 5 V supply to the PDM output stage.

> Note: Sequence steps are only available when a measurement is run with the sequencer in the Measurement Navigator.

Clock-Switch Recovery for Jitter Level Sweep and Jitter Frequency Sweep

Jitter Level Sweep and **Jitter Frequency Sweep** measurements automatically enable the jitter generator when the measurement context occurs, before the Sequence Steps shown in Figure 35. This means that if the **Signal Path Setup Clocks** panel was set with Jitter Generator **OFF**, the PDM interface will switch to a jittered clock, momentarily stopping the bit clock, resulting in a reset to the PDM part.

To recover from the PDM device reset caused by the clock switch, send the PDM control code before the Measure sequence step, as shown by red arrows in Figure 35.

Clock-Switch Recovery for Nested Jitter Measurements

Measurements with optional nested sweeps (**Acoustic Response, Continuous Sweep, Frequency Response,** and **Signal Analyzer**) allow the nested sweep source to be jitter level or jitter frequency. When jitter is selected as a nested sweep source, clock switching occurs during the **Measurement** sequence step. This means PDM control codes sent before the **Measure** sequence step will be reset.

Avoid this by enabling the **Jitter Generator** in the **Signal Path Clocks** panel and setting the **Jitter Peak Level** value to **0.0**. This switches the signal path to the jittered clock before any measurements can be executed. All APx measurements in the signal path will have no jitter except jitter sweep measurements that set the jitter level above 0. A clock switch will never occur during sequence execution; PDM control codes sent during sequence execution will not be reset.

Maximum Bit Clock Rate vs. Logic Levels

The PDM input and output interfaces share a common logic level setting. The maximum clock rate of the PDM interface is automatically limited by the logic level setting in order to assure error-free operation of the APx PDM interface at all logic levels.

The table below defines the maximum bit clock frequency limit. Interpolation ratio and Decimated Rate settings will be limited to prevent bit clock rates exceeding the values in the table.

Logic Level Minimum	Logic Level Maximum	Maximum Clock Frequency
0.8 V	< 1.0 V	3.072 MHz
1.0 V	< 1.5 V	6.144 MHz
1.5 V	< 2.0 V	12.288 MHz
2.0 V	3.3 V	24.576 MHz

Set the **Logic Level** before all other PDM interface settings to minimize interaction between **Decimated Rate** and **Interpolation** ratio settings.

Lowering the logic level on a PDM settings panel to a different range may automatically reduce the **Decimated Rate** (sample rate) and leave the **Interpolation** ratio unchanged.

Sample APx Projects

A sample APx project file for PDM amplifier testing is available with this Technote. The project measures audio performance and jitter tolerance with Sequence Mode. It performs measurements with methods discussed in this Technote. Use this as a starting point for your projects.

File Name:

Class D Amplifier PDM Input to Spkr Out, Audio Performance & Jitter Tolerance.approjx

References:

APx PDM Option
http://www.ap.com/products/apx/pdm

APx PDM Datasheet
http://www.ap.com/display/file/614

Understanding PDM Digital Audio
http://www.ap.com/display/file/612

PDM Option Technical Details
http://www.ap.com/display/file/619

PDM Line Driver
http://www.ap.com/products/accessories/pdmdrvr

PDM Line Driver Users Guide
http://www.ap.com/display/file/684

CAB-PDM description: (PDM cable for APX-PDM option)
http://www.ap.com/display/file/638

TN117: Measuring PDM Microphones and Inputs with APx
http://www.ap.com/display/file/624

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